CLAIMS

We claim:

1. A process for manufacturing a phase change memory cell, comprising the steps of:

forming a resistive element;

forming a delimiting structure having an aperture over said resistive element; and

forming a memory portion of a phase change material in said aperture, said resistive element and said memory portion being in direct electrical contact and defining a contact area of sublithographic extension;

wherein said step of forming said memory portion comprises filling said aperture with said phase change material and removing from said delimiting structure any portion of said phase change material exceeding said aperture.

2. A process according to claim 1, wherein said step of removing is followed by the step of sealing said memory portion inside said aperture.

3. A process according to claim 2, wherein said step of sealing comprises depositing a sealing structure directly on said delimiting structure.

4. A process according to claim 1, wherein said step of filling said aperture comprises depositing a memory layer on said delimiting structure.

5. A process according to claim 4, wherein said step of forming said delimiting structure comprises depositing at least a dielectric layer.

6. A process according to claim 5, wherein said step of filling comprises depositing said memory layer directly on said dielectric layer.

7. A process according to claim 5, wherein, before said step of filling, an adhesion layer is deposited on said dielectric layer.

8. A process according to claim 7, wherein said step of removing further comprises completely removing said adhesion layer.

9. A process according to claim 1, wherein said resistive element includes a first thin portion having a first sublithographic dimension in a first direction and said memory portion has a second sublithographic dimension in a second direction transverse to said first direction; said contact area of sublithographic extension having substantially said first sublithographic dimension in said first direction and said second sublithographic dimension in said second direction.

10. A phase change memory cell, comprising:

a resistive element;

a delimiting structure, having an aperture over said resistive element; and

a memory portion of a phase change material, housed in said aperture, said resistive element and said memory portion being in direct electrical contact and defining a contact area of sublithographic extension;

wherein said memory portion is sealed inside said aperture by a sealing structure directly lying on said delimiting structure.

11. A phase change memory cell according to claim 10, wherein said delimiting structure comprises at least a dielectric layer.

12. A phase change memory cell according to claim 11, wherein said sealing structure lies directly on said dielectric layer.

13. A phase change memory cell according to claim 11, wherein said delimiting structure comprises adhesion portions interposed between said dielectric layer and said sealing structure.

14. A phase change memory cell according to claim 10, wherein said memory portion is aligned with said delimiting structure.

15. A phase change memory cell according to claim 10, wherein said sealing structure comprises a stack of conducting layers.

16. A phase change memory cell according to claim 10, wherein said resistive element includes a first thin portion having a first sublithographic dimension in a first direction and said memory portion has a second sublithographic dimension in a second direction transverse to said first direction; said contact area of sublithographic extension having substantially said first sublithographic dimension in said first direction and said second sublithographic dimension in said second direction.

17. The memory cell according to claim 10, wherein said memory portion has a substantially elongated shape with a main dimension extending parallel to said first direction.

18. A process according to claim 1 wherein said aperture is a slit.

19. A phase change memory cell according to claim 10 wherein said aperture is a slit.

20. A memory device comprising:

a selection element; and

a phase change memory element coupled to said selection element, said phase change memory element having a resistive element; a delimiting structure having an aperture over said resistive element; and a memory portion of a phase change material, housed in said aperture, said resistive element and said memory portion being in direct electrical contact and defining a contact area of sublithographic extension, wherein said memory portion is sealed inside said aperture by a sealing structure directly lying on said delimiting structure.

21. A memory device according to claim 20 wherein said selection element is a transistor.

22. A memory device according to claim 20 wherein said selection element is a diode.

23. A memory device according to claim 20 wherein said aperture is a slit.

24. A memory device comprising:

first resistive element;

second resistive element;

delimiting structure with an aperture having first portion over first resistive element and second portion over second resistive element;

first memory portion of phase change material in first portion of said aperture, the first resistive element and first memory portion together forming a first memory element, and

second memory portion of phase change material in second portion of said aperture, the second resistive element and second memory portion together forming a second memory element.

25. The memory device according to claim 24 wherein said first and second memory portions are sealed inside said aperture by a sealing structure directly lying on said delimiting structure.

26. The memory device according to claim 24 wherein said aperture is a slit.